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09/751979
12/29/00

438	714
Class	Subclass
ISSUE CLASSIFICATION	

U.S. UTILITY Patent Application

O.I.P.E.		PATENT DATE
SCANNED	8/30	O.A. 1C

PATENT NUMBER

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/751979	F	438	714	1763	Goudreau

Applicant's Name: Akiushi Nishizawa

TITLE
Manufacturing method, semiconductor integrated circuit including simultaneous formation of via hole, rearward metal wiring and concave groove in interlayer film and semiconductor integrated circuit manufactured with the manufacturing method

PTO-2040
12/99

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ISSUING CLASSIFICATION								
ORIGINAL		CROSS REFERENCE(S)						
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
438	714	438	725	717	723	724	736	743
INTERNATIONAL CLASSIFICATION		430	5					
H01L 21/302		438	751	749	734			
<input type="checkbox"/> Continued on Issue Slip Inside File Jacket								

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
	6	20	70	10	1
NOTICE OF ALLOWANCE MAILED					
8-12-03					
ISSUE FEE					
			Amount Due	Date Paid	
			\$1,600		
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.				ISSUE BATCH NUMBER	
				M. Waugh 8/13/03	
(Legal Instruments Examiner) (Date)					

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